

IN THE CLAIMS

What is claimed is:

- 1 **1.** A semiconductor device, comprising:
 - 2 a low resistance embedded wiring layer formed on and extending over
 - 3 a semiconductor substrate; and
 - 4 a plurality of element regions formed over the embedded wiring layer
 - 5 separated from one another and having at least one circuit element formed
 - 6 therein, each element region being in contact with the embedded wiring layer.

- 1 **2.** The semiconductor device of claim 1, wherein:
 - 2 the plurality of element regions includes at least one supply element
 - 3 region in contact with the embedded wiring layer and receiving a
 - 4 predetermined power source potential.

- 1 **3.** The semiconductor device of claim 1, further including:
 - 2 an insulating layer formed between the embedded wiring layer and the
 - 3 semiconductor substrate;
 - 4 the embedded wiring layer is electrically connected to the
 - 5 semiconductor substrate through at least one opening in the insulating layer;
 - 6 and
 - 7 the semiconductor substrate receives a predetermined power source
 - 8 potential.

1 **4.** The semiconductor device of claim 1, wherein:

2 the at least one circuit element includes a transistor having a source
3 region, drain region, and channel region formed in the element region, the
4 channel region being situated between each of the source and drain regions
5 and the embedded wiring layer.

1 **5.** The semiconductor device of claim 1, wherein:

2 the least one circuit element includes a transistor having a source
3 region, drain region, and channel region formed in the element region, the
4 channel region being situated between one of the source and drain regions,
5 and the other of the source and drain regions being electrically connected to
6 the embedded wiring layer.

1 **6.** The semiconductor device of claim 1, wherein:

2 the least one circuit element includes a transistor having a source
3 region, drain region, and channel region formed in the element region, the
4 element region being surrounded by at least one insulating layer except for
5 a bottom portion thereof, the source and drain regions being in contact
6 with the at least one insulating layer and not in contact with the embedded
7 wiring layer.

1 **7.** A semiconductor device, comprising:

2 a low resistance first embedded wiring layer and a low resistance
3 second embedded wiring layer both formed on and extending over a
4 semiconductor substrate, the first embedded wiring layer supplied with a first
5 potential and the second embedded wiring layer supplied with a second
6 potential different than the first potential;

7 a plurality of first element regions in contact with the first embedded
8 wiring layer, each having at least one circuit element formed therein; and

9 a plurality of second element regions in contact with the second
10 embedded wiring layer, each having at least one circuit element formed
11 therein.

1 **8.** The semiconductor device of claim 7, wherein:

2 the plurality of first element regions includes at least one first supply
3 element region in contact with the first embedded wiring layer and receiving
4 the first potential; and

5 the plurality of second element regions includes at least one second
6 supply element region in contact with the second embedded wiring layer and
7 receiving the second potential.

1 **9.** The semiconductor device of claim 7, further including:

2 an insulating layer formed between the first and second embedded
3 wiring layers and the semiconductor substrate;

4 the first potential is supplied to at least one first supply element region

5 in contact with the first embedded wiring; and
6 the second embedded wiring layer is electrically connected to the
7 semiconductor substrate through at least one opening in the insulating layer,
8 and the semiconductor substrate receives the second potential.

1 **10.** The semiconductor device of claim 7, wherein:

2 the at least one circuit element formed in the plurality of first element
3 regions comprises a first conductivity type transistor; and

4 the at least one circuit element formed in the plurality of second
5 element regions comprises a second conductivity type transistor.

1 **11.** The semiconductor device of claim 7, wherein:

2 the first embedded wiring layer is connected to a bottom surface of at
3 least one first element region through bottom contact holes formed through a
4 bottom insulating layer and a top wiring is connected to a top surface of the at
5 least one first element region through top source/drain contact holes aligned
6 over the bottom contact holes.

1 **12.** The semiconductor device of claim 7, wherein:

2 the at least one circuit element formed in the plurality of first element
3 regions comprises a field effect transistor having a first source/drain region, a
4 second source/drain region, and a channel region; and

5 the first embedded wiring layer contacts the first source/drain region

6 and the channel region, and does not contact the second source/drain region.

1 13. The semiconductor device of claim 7, wherein:

2 at least one circuit element formed in the plurality of first element
3 regions comprises a field effect transistor having a first source/drain region, a
4 second source/drain region, and a channel region, the first and second
5 source/drain regions extending from a top surface of the first element region
6 to a bottom surface of the first element region; and

7 the first embedded wiring layer contacts the channel region, and does
8 not contact the first or second source/drain regions.

1 14. The semiconductor device of claim 7, wherein:

2 the low resistance first embedded wiring layer and the low resistance
3 second embedded wiring layer comprise a metal.

1 15. A method of manufacturing a semiconductor device, comprising the steps of:

2 forming a silicon-on-insulator (SOI) type substrate that includes a first
3 semiconductor substrate, a first insulating film formed over the semiconductor
4 substrate, and a semiconductor layer formed over the first insulating film;

5 forming at least one insulated gate field effect transistor (IGFET) in a
6 portion of the semiconductor layer separated from other portions of the
7 semiconductor layer by isolation regions of the SOI type substrate;

8 planarizing the first semiconductor substrate to expose the first

9 insulating film;
10 removing at least a portion of the first insulating layer to expose the
11 semiconductor layer;
12 forming a first conductive layer in contact with the first insulating film
13 and the semiconductor layer;
14 forming a second conductive layer on a second semiconductor
15 substrate;
16 bonding the SOI type substrate to the second semiconductor substrate
17 with the first conductive layer in contact with the second conductive layer;
18 and
19 heat treating the SOI type substrate and the second semiconductor
20 substrate to fuse the first conductive layer to the second conductive layer.

1 **16.** The method of claim 15, further including:

2 patterning the first conductive layer to form a first wiring;
3 forming a second insulating film that covers the first insulating layer
4 and the first wiring, and planarizing the resulting surface to expose the first
5 wiring;
6 patterning the second conductive layer to form a second wiring;
7 forming a fourth insulating film that covers the second insulating layer
8 and second wiring, planarizing a resulting surface to expose the second
9 wiring;
10 bonding the SOI type substrate to the second semiconductor substrate

11 includes bonding the first wiring to the second wiring; and
12 heat treating the SOI type substrate and the second semiconductor
13 substrate fuses the first wiring to the second wiring.

1 17. The method of claim 15, wherein:

2 forming the at least one IGFET includes etching holes through a top
3 insulating films with a source/drain contact hole mask; and
4 removing at least a portion of the first insulating layer to expose the
5 semiconductor layer includes etching through the first insulating layer with a
6 mask developed from the source/drain contact hole mask.

1 18. The method of claim 15, wherein:

2 the other portions of the semiconductor layer include at least one
3 supply portion coupled to a power source potential.

1 19. The method of claim 15, wherein:

2 forming the SOI type substrate includes
3 oxidizing a surface of the first semiconductor substrate,
4 oxidizing a surface of a third semiconductor substrate,
5 bonding the oxidized surface of the first semiconductor
6 substrate to the oxidized surface of the third semiconductor substrate,
7 and
8 planarizing the third semiconductor substrate to form the

9 semiconductor layer.

1 20. The method of claim 15, wherein:

2 forming the SOI type substrate includes implanting oxygen into a
3 semiconductor substrate to form the first insulating film of silicon oxide, the
4 portion of the semiconductor substrate below the first insulating film being the
5 first semiconductor substrate, the portion of the semiconductor substrate
6 above the first insulating film being the semiconductor layer.